IN THE CLAIMS:

Please cancel claims 1, 3, 4, 13-16 and 21, and amend the claims as follows:

1. (Canceled)

2. (Currently Amended) The method as claimed in claim [[1]] 22, wherein method steps a) to c) are repeated and different semiconductor chips are selected in method step a) in [[the]] a course of two cycles taking place at successive times[[;]].

3. (Canceled)

4. (Canceled)

5. (Currently Amended) The method as claimed in claim [[4]] 23, wherein the statistical method takes into account ~~the~~ at least one of an arrangement of the semiconductor chips on the modules ~~and/or the~~ and an arrangement of the modules in relation to one another or in relation to one or more other adjacent components[[;]].

6. (Currently Amended) The method as claimed in claim [[4]] 23, wherein the statistical method takes into account at least one of empirically obtained ~~and/or~~ and currently ascertained data[[;]].

7. (Currently Amended) ~~The method as claimed in claim 1,~~A method for operating semiconductor chips, particularly memory chips, which are arranged in groups on modules which are connected to a common data bus, wherein each semiconductor chip on each module is connected to at least one data line in the common data bus, comprising the following method steps:

a) selecting a group of semiconductor chips from the semiconductor chips arranged on the modules based on a prescribed selection criterion independently of module, the selected group of semiconductor memory chips using data lines in the common data bus over the entire bus width;

b) activating the semiconductor chips in the selected group; and

c) performing data interchange between the data lines in the common data bus and the selected group of semiconductor chips;

wherein each of the semiconductor chips has an associated selection probability[[;]].

8. (Currently Amended) The method as claimed in claim 7,

wherein the semiconductor chips are arranged in three dimensions with respect to one another; and

wherein the associated selection probability for a semiconductor chip depends on its relative situation with respect to adjacent semiconductor chips, and wherein a semiconductor chip in an outer region of the modules has a higher selection probability than a semiconductor chip in an inner region[[;]].

9. (Currently Amended) ~~The method as claimed in claim 1,~~A method for operating semiconductor chips, particularly memory chips, which are arranged in groups on modules which are connected to a common data bus, wherein each semiconductor chip on each module is connected to at least one data line in the common data bus, comprising the following method steps:

a) selecting a group of semiconductor chips from the semiconductor chips arranged on the modules based on a prescribed selection criterion independently of module, the selected group of semiconductor memory chips using data lines in the common data bus over the entire bus width;

b) activating the semiconductor chips in the selected group; and

c) performing data interchange between the data lines in the common data bus and the selected group of semiconductor chips;

wherein each of the semiconductor chips arranged on the modules has an associated individual index which denotes [[the]] a corresponding module and [[the]] a position of the corresponding semiconductor chip on the corresponding module;

wherein associated [[the]] indices for the group of semiconductor chips which was selected independently of the modules in method step a) are stored in a register device; and

wherein the associated indices for the semiconductor chips associated with [[the]] a corresponding group are read from the register device in method step b) and the corresponding semiconductor chips are activated using their associated indices[[;]].

10. (Currently Amended) The method as claimed in claim [[1]] 23,

wherein method steps a) to c) take place at the beginning of a startup procedure in which the semiconductor chips are started up[[;]].

11. (Currently Amended) The method as claimed in claim [[1]] 23,

wherein the semiconductor chips are memory chips, and

wherein the method steps a) to c) take place at a time at which the content of the memory chips is redundant[[;]].

12. (Currently Amended) The method as claimed in claim [[1]] 23,

wherein the semiconductor chips are memory chips, and

wherein [[the]] data already stored in the memory chips are stored in a buffer store before a group of memory chips is selected in method step a)[[;]].

13.-16. (Canceled)

17. (Currently Amended) ~~The control apparatus as claimed in one of claims 14,~~ A control apparatus for operating semiconductor chips, particularly memory chips, which are arranged in groups on modules which are connected to a common data bus;

wherein each semiconductor chip on each module is connected to at least one data line in the common data bus, comprising:

a selection device for selecting the semiconductor chips for a group cyclically based on a prescribed selection criterion independently of module; and

an activation device for activating the semiconductor chips in the selected group for data interchange with data lines in the common data bus;

wherein the selection device is ~~designed in order~~ configured to assign each semiconductor chip an individual selection probability based on ~~the basis of~~ its relative situation in a three-dimensional arrangement of the semiconductor chips[[;]].

18. (Currently Amended) ~~The control apparatus as claimed in claim 14,~~ A control apparatus for operating semiconductor chips, particularly memory chips, which are arranged in groups on modules which are connected to a common data bus;

wherein each semiconductor chip on each module is connected to at least one data line in the common data bus, comprising:

a selection device for selecting the semiconductor chips for a group cyclically based on a prescribed selection criterion independently of module;

an activation device for activating the semiconductor chips in the selected group for data interchange with data lines in the common data bus; and

[[where]] an assessment device ~~is designed in order to assess~~ for assessing the semiconductor chips according to prescribed criteria, particularly [[the]] a temperature of the semiconductor chips, and

wherein the selection device is ~~designed in order~~ configured to select the semiconductor chips based on ~~the basis of the~~ assessment results from the assessment device[[;]].

19. (Currently Amended) ~~The control apparatus as claimed in claim 14,~~ A control apparatus for operating semiconductor chips, particularly memory chips, which are arranged in groups on modules which are connected to a common data bus;

wherein each semiconductor chip on each module is connected to at least one data line in the common data bus, comprising:

a selection device for selecting the semiconductor chips for a group cyclically based on a prescribed selection criterion independently of module; and

an activation device for activating the semiconductor chips in the selected group for data interchange with data lines in the common data bus;

wherein the activation device is ~~designed in order~~ configured to activate the semiconductor chips in [[the]] an active group using an index which is individually associated with each of the semiconductor chip and denotes [[the]] a corresponding module and [[the]] a position of [[the]] a corresponding semiconductor chip[[;]].

20. (Currently Amended) ~~The control apparatus as claimed in claim 14,~~ A control apparatus for operating semiconductor chips, particularly memory chips, which are arranged in groups on modules which are connected to a common data bus;

wherein each semiconductor chip on each module is connected to at least one data line in the common data bus, comprising:

a selection device for selecting the semiconductor chips for a group cyclically based on a prescribed selection criterion independently of module;

an activation device for activating the semiconductor chips in the selected group for data interchange with data lines in the common data bus; and

[[where]] a register device ~~is designed in order to store~~ for storing the information about [[the]] an association between the semiconductor chips and [[the]] an active group of semiconductor chips[[;]].

21. (Canceled)

Please add the following new claims:

22. (New) A method for operating semiconductor chips, particularly memory chips, which are arranged in groups on modules which are connected to a common data bus, wherein each semiconductor chip on each module is connected to at least one data line in the common data bus, comprising the following method steps:

a) selecting a group of semiconductor chips from the semiconductor chips arranged on the modules based on a prescribed selection criterion independently of

module, the selected group of semiconductor memory chips using data lines in the common data bus over the entire bus width;

b) activating the semiconductor chips in the selected group; and

c) performing data interchange between the data lines in the common data bus and the selected group of semiconductor chips;

wherein the prescribed selection criterion is a temperature of the semiconductor chips and wherein semiconductor chips having the lowest temperature are selected.

23. (New) A method for operating semiconductor chips, particularly memory chips, which are arranged in groups on modules which are connected to a common data bus, wherein each semiconductor chip on each module is connected to at least one data line in the common data bus, comprising the following method steps:

a) selecting a group of semiconductor chips from the semiconductor chips arranged on the modules based on a prescribed selection criterion independently of module, the selected group of semiconductor memory chips using data lines in the common data bus over the entire bus width;

b) activating the semiconductor chips in the selected group; and

c) performing data interchange between the data lines in the common data bus and the selected group of semiconductor chips;

wherein the semiconductor chips are selected using a statistical method.

24. (New) A method for operating semiconductor chips, particularly memory chips, which are arranged in groups on modules which are connected to a common data bus, wherein each semiconductor chip on each module is connected to at least one data line in the common data bus, comprising the following method steps:

a) selecting a group of semiconductor chips from the semiconductor chips arranged on the modules based on a prescribed selection criterion independently of module, the selected group of semiconductor memory chips using data lines in the common data bus over the entire bus width;

b) activating the semiconductor chips in the selected group; and

c) performing data interchange between the data lines in the common data bus and the selected group of semiconductor chips;

wherein, besides the group of semiconductor chips which is selected in method step a), a further group of further semiconductor chips is selected independently of module, and the semiconductor chips in this further group likewise use the data lines in the common data bus over the entire bus width, and

wherein the data interchange between the data lines in the data bus and the semiconductor chips in the group selected in method step c) involves alternating between groups of semiconductor chips.

25. (New) A control apparatus for operating semiconductor chips, particularly memory chips, which are arranged in groups on modules which are connected to a common data bus;

wherein each semiconductor chip on each module is connected to at least one data line in the common data bus, comprising:

a selection device for selecting the semiconductor chips for a group cyclically based on a prescribed selection criterion independently of module; and

an activation device for activating the semiconductor chips in the selected group for data interchange with data lines in the common data bus;

wherein the selection device is configured to select the semiconductor chips for an active group based on a temperature of the semiconductor chips.

26. (New) A control apparatus for operating semiconductor chips, particularly memory chips, which are arranged in groups on modules which are connected to a common data bus;

wherein each semiconductor chip on each module is connected to at least one data line in the common data bus, comprising:

a selection device for selecting the semiconductor chips for a group cyclically based on a prescribed selection criterion independently of module; and

an activation device for activating the semiconductor chips in the selected group for data interchange with data lines in the common data bus;

wherein the selection device is configured to select the semiconductor chips for an active group using a statistical method.